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**OPTICAL TRANSMISSION SYSTEM FOR  
COMPENSATING FOR TRANSMISSION LOSS**

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an optical transmission system, and more particularly, to an optical transmission system for compensating for transmission loss, an optical signal transmitting/receiving apparatus of the optical transmission system for compensating for transmission loss, and a parallel/serial data converter for transmitting high speed data in the transmitting apparatus.

2. Description of the Related Art

An optical transmission system includes an optical signal transmitting apparatus, an optical fiber, and an optical signal receiving apparatus. The transmitting apparatus converts an electrical signal to be transmitted into an optical signal, using a laser diode. The optical fiber transmits the optical signal converted by the transmitting apparatus to a receiving apparatus. The receiving apparatus receives the optical signal transmitted through the optical fiber at a photo diode and converts the received signal into an electrical signal.

The transmitting apparatus provides driving current to the laser diode in order to output the optical signal using the laser diode. Namely, the transmitting apparatus controls the driving current and controls the optical output power of the laser diode. Conventional transmitting apparatus commonly control the amount of driving current by controlling an external resistance value.

FIG. 1 is a schematic block diagram showing a conventional single channel optical signal transmission system. Referring to FIG. 1, a transmitting apparatus 10 includes an optical driver 12, a bias and modulation current controller 14, a bias resistor  $R_{bias}$ , a modulation resistor  $R_{mod}$ , and a laser diode 16. A receiving apparatus 20 includes an optical receiver 26 and a photo diode 24. Here, the bias resistor  $R_{bias}$  and the modulation resistor  $R_{mod}$  can exist outside the transmitting apparatus 10.

In FIG. 1, the optical driver 12 of the transmitting apparatus 10 converts externally-received input data DIN into a current signal. The optical driver 12 further changes the magnitude of the converted current signal in response to the bias current  $I_{bias}$  and the modulation current  $I_{mod}$ , which are provided by the bias and modulation current controller 14. The magnitudes of the bias current  $I_{bias}$  and the modulation current  $I_{mod}$  can be controlled by changing the magnitudes of the bias resistor  $R_{bias}$  and the modulation resistor  $R_{mod}$ . Also, the optical driver 12 generates a magnitude-variant current signal as the driving current for driving the laser diode 16. The laser diode 16 generates an optical signal having an optical output power corresponding to the driving current. The optical signal generated by the laser diode 16 is transmitted to the receiving apparatus 20 through an optical fiber 18. The photo diode 24 of the receiving apparatus 20 receives the optical signal transmitted from the optical fiber 18 and converts the received optical signal into a current signal. The optical receiver 26 recovers original data from the current signal converted by the photo diode 24. In FIG. 1, DOUT represents recovered data.

The conventional optical transmission system shown in FIG. 1 controls the amount of driving current  $I_d$  output from the optical driver 12 by changing the magnitudes of the bias resistor  $R_{bias}$  and the modulation resistor  $R_{mod}$ , thus controlling the magnitudes of the bias current  $I_{bias}$  and the modulation current  $I_{mod}$ . Namely, the optical output power of the laser diode 16 is controlled by changing the resistances of the bias resistor  $R_{bias}$  and the modulation resistor  $R_{mod}$ .

The conventional optical transmission system shown in FIG. 1 is an open loop system, in which the optical output power of the laser diode 16 can be controlled only at the transmission end.

For example, when transmission loss is generated while the optical signal is transmitted through the optical fiber, or received by the receiving apparatus, errors can be generated in the data recovered by the optical receiver of the receiving apparatus. Therefore, the transmitting apparatus transmits an optical signal having appropriate optical output power so that the optical transmission system can maintain a

predetermined transmission efficiency, taking into account transmission loss. The transmission efficiency can change according to the characteristics of the devices used for the optical transmission system such as the optical diodes for transmission, the optical fibers, and the optical diodes for reception. Also, the transmission efficiency of the optical transmission system can change as the length of the optical fiber changes. Also, the transmission efficiency of the optical transmission system can change since the characteristics of the devices used as the optical fiber may not optimally match. Transmission loss can be different from what was expected due to the change in the transmission efficiency. Accordingly, errors can be generated in the data recovered by the optical receiver of the receiving apparatus.

Also, in the case of a multi-channel optical transmission system for transmitting multimedia data such as graphic data, uniformities of the laser diode, the optical fiber and the photo diode can vary in each channel. Therefore, in the case of the multi-channel optical transmission system, transmission efficiency varies in each channel. Accordingly, errors can be generated when data is transmitted.

In the conventional open-loop optical transmission system, the optical output power is controlled according to the characteristics of the transmitting apparatus. However, the change in transmission efficiency according to the characteristics of the optical fiber and the receiving apparatus is not taken into account. Namely, the transmission efficiency changes due to the characteristics of the optical fiber and the receiving apparatus. Accordingly, it is not possible to compensate for errors generated when data is transmitted.

Also, in order to minimize the change in transmission efficiency caused by the characteristics of the optical fiber and the receiving apparatus, the error allowance range of the standards of the devices used for the optical transmission system must be small. Therefore, when the conventional optical transmission system of the open loop is constituted, restrictions are placed on selection of the devices. Accordingly, it is expensive to constitute the optical transmission system.

## SUMMARY OF THE INVENTION

To address the above issues, it is an object of the present invention to provide an optical transmission system for compensating for transmission loss so that the transmission efficiency of an optical transmission system is kept uniform regardless of the characteristics of an optical fiber and a receiving apparatus.

It is another object of the present invention to provide a transmitting apparatus for an optical transmission system for compensating for transmission loss.

It is another object of the present invention to provide a receiving apparatus for an optical transmission system for compensating for transmission loss.

It is another object of the present invention to provide a parallel/serial data converting circuit for transmitting data at high speed in the transmitting apparatus for optical transmission.

Accordingly, to achieve the first object, according to an aspect of the present invention, there is provided an optical transmission system for compensating for transmission loss, comprising a transmitting apparatus for serializing a plurality of  $n$ -bit (where  $n$  is a natural number), externally-received channel data in response to a predetermined clock signal, converting the serialized channel data into a first current signal and the predetermined clock signal into a second current signal whose magnitudes change in accordance with an error detection signal, and outputting optical signals having optical output power corresponding to the magnitudes of the current signals, a first optical fiber for transmitting the optical signals, a receiving apparatus for recovering the  $n$ -bit channel data and the predetermined clock signal from the optical signals received through the optical fibers, detecting transmission loss generated when the optical signals are transmitted and received, optically converting the transmission loss, and outputting the optically converted transmission loss as the error detection signal, and a second optical fiber for transmitting the converted error detection signal to the transmitting apparatus.

To achieve the first object, according to another aspect of the present invention, there is provided an optical transmission system for compensating for transmission

loss, comprising a transmitting apparatus for serializing a plurality of externally-received n-bit channel data in response to a predetermined clock signal, converting the serialized channel data and the predetermined clock signal into first and second current signals whose magnitudes change in accordance with an error detection signal, and outputting optical signals having optical output power corresponding to the magnitude of the current signals, optical fibers for transmitting the optical signals, a receiving apparatus for recovering the n-bit channel data and the predetermined clock signal from optical signals received by the optical fibers and outputting transmission loss generated when the optical signals are transmitted and received as the error detection signal, and an electrical transmission line for transmitting the error detection signal to the transmitting apparatus.

To achieve the second object, according to an aspect of the present invention, there is provided a transmitting apparatus for receiving transmission loss detected by an external receiving apparatus through a first optical fiber and transmitting a plurality of channel data items to the receiving apparatus through a second optical fiber, comprising a PLL for generating a clock signal synchronized with a predetermined clock signal received from the outside and outputting the synchronized clock signal as an actual clock signal for transmitting data, a parallel/serial data converter for receiving a plurality of external n-bit channel data in response to the synchronized clock signal and serializing the n-bit channel data in response to the synchronized clock signal, an optical diode for reception for converting an error detection signal transmitted from the first optical fiber into a current signal and outputting the current signal, an error compensating driver for converting channel data serialized by the parallel/serial data converter and the synchronized clock signal into current signals, changing the magnitudes of the converted current signals, corresponding to the current signal converted by the optical diode for reception, and outputting the current signals as driving signals, and a plurality of optical diodes for transmission for outputting optical signals having optical output power corresponding to the driving signals.

To achieve the third object, according to an aspect of the present invention, there is provided a receiving apparatus for receiving channel data items transmitted from an external transmitting apparatus through an optical fiber and recovering the channel data items from a received optical signal, comprising a plurality of optical diodes for reception of external optical signals and converting the optical signals into current signals, an error detection unit for converting the current signals converted by the plurality of optical diodes for reception into voltage signals, digitizing the voltage signals, outputting the digitized voltage signals as recovered serial channel data and a recovered clock signal, detecting transmission loss of each channel from the voltage signals, encoding the transmission loss, converting the encoded transmission loss into current, and outputting the current, a PLL for generating a synchronized clock signal synchronized with the recovered clock signal and outputting the synchronized clock signal as an actual clock signal for receiving data, a data recovery unit for recovering the recovered serial channel data to n-bit parallel data in response to the synchronized clock signal, and an optical diode for transmission for converting the signal encoded and inverted into current by the error detection unit into an optical signal.

To achieve the fourth object, according to an aspect of the present invention, there is provided a parallel/serial data converting circuit of a transmitting apparatus, comprising a phase locked loop (PLL) for generating first through nth overlapping clock signals having a predetermined offset so as not to overlap each other and inverted first through nth overlapping clock signals by inverting the first through nth overlapping clock signals, the parallel/serial data converting circuit for converting channel data items of n bit, which are input from an external source, into serial information data in response to the first through nth overlapping clock signals and transmitting the converted data, comprising a data latch for receiving the n-bit channel data and segmenting the received n-bit channel data by N bits and latching the segmented channel data in response to first through mth latch clock signals and a data serializer for performing a logic operation on the n-bit channel data latched by the data latch, the first through nth

non-overlapping clock signal and the inverted first through nth non-overlapping clock signal and outputting the logic operation result as serial channel data.

BRIEF DESCRIPTION OF THE DRAWING(S)

The above objects and advantages of the present invention will become more apparent by describing in detail a preferred embodiment thereof with reference to the attached drawings in which:

FIG. 1 is a schematic block diagram showing a conventional single channel optical signal transmission system;

FIG. 2 is a schematic block diagram showing an optical transmission system for compensating for transmission loss according to an embodiment of the present invention;

FIG. 3 is a block diagram showing a phase locked loop (PLL) 140 shown in FIG. 2;

FIG. 4 is a circuit diagram showing a voltage controlled oscillator (VCO) 146 shown in FIG. 3;

FIG. 5 shows waveforms of first through ninth non-overlapping clock signals and a first synchronized clock signal, which are output from the VCO shown in FIG. 4;

FIG. 6 is a block diagram showing the parallel/serial data converter 110 shown in FIG. 2;

FIGS. 7A and 7B show waveforms of the operation of the apparatus shown in FIG. 6;

FIG. 8 is a circuit diagram showing the latch 700 shown in FIG. 6;

FIGS. 9A through 9H show main waveforms of the operation of the data latch shown in FIG. 8;

FIG. 10 is a circuit diagram showing the data serializer 750 shown in FIG. 6;

FIG. 11 is a block diagram showing the error compensating driver 160 shown in FIG. 2;

FIG. 12 is a block diagram showing the transmission error compensator 164 shown in FIG. 11;

FIG. 13 is a block diagram showing the error detection unit 210 shown in FIG. 2;

FIG. 14 is a block diagram showing an embodiment of the transmission error detector 222 shown in FIG. 13; and

FIG. 15 is a block diagram showing another embodiment of the transmission error detector 222 shown in FIG. 13.

#### DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

FIG. 2 is a schematic block diagram showing an optical transmission system for compensating for transmission loss according to an embodiment of the present invention. The optical transmission system includes a transmitting apparatus 100, first and second optical fibers 185 and 195, and a receiving apparatus 200. The second optical fiber 195 can be replaced by an electrical transmission line 193. In the present specification, the optical transmission system using the second optical fiber 195 will be described.

The transmitting apparatus 100 serializes n-bit channel data items received from an external source in response to a predetermined clock signal CLK. The transmitting apparatus 100 converts the serialized channel data items and predetermined clock signal CLK into optical signals and outputs the optical signals. The transmitting apparatus 100 can change the output power of the respective optical signals output from the transmitting apparatus 100 in response to an error detection signal transmitted through the second optical fiber 195. In an embodiment of the present invention, for the convenience of explanation, n-bit channel data items are R/G/B color signals and a control signal CON. Also, the transmitting apparatus 100 inputs the R/G/B color signals and the control signal CON through input terminals R\_IN, G\_IN, B\_IN, and CON\_IN, respectively. Also, the predetermined clock signal CLK is received through an input terminal CLK\_IN. The control signal CON includes horizontal/vertical synchronous signals HSYNC and VSYNC and a data enable signal DE.



The R/G/B color signals and the control signal CON input to the transmitting apparatus 100 can be data scrambled by an external scrambler. Here, in the scrambled data, the number of high levels and low levels of digital data input in response to the predetermined clock signal CLK is counted and the count is added to the respective channel data items as direct current (DC) balance information. Namely, direct current balance information added by the scrambler shows that the high levels and the low levels of the respective data bits are well-balanced in digital transmission. The DC balance information determines the level of data when data is recovered by a receiver. In the present specification, for convenience of explanation, the R/G/B color signal and the control signal CON input to the transmitting apparatus 100 are scrambled data of nine bits.

A first optical fiber 185 transmits an optical signal output from the transmitting apparatus 100 to a receiving apparatus 200.

The receiving apparatus 200 receives optical signals transmitted from the first optical fiber 185 and recovers the R/G/B color signals and the control signal CON of n bits which are original digital signals and the predetermined clock signal CLK. In FIG. 2, R\_OUT, G\_OUT, B\_OUT, and CON\_OUT denote the recovered R/G/B color signals and control signal and CLK\_OUT denotes the recovered predetermined clock signal. Also, the receiving apparatus 200 detects transmission loss generated when the optical signals output from the transmitting apparatus 100 to the respective channels are transmitted through the first optical fiber 185 and when the optical signals are received by the receiving apparatus 200. The receiving apparatus 200 converts the detected transmission loss into an optical signal and outputs the converted optical signal as an error detection signal.

A second optical fiber 195 transmits the error detection signal output from the receiving apparatus 200 to the transmitting apparatus 100.

The optical transmission system according to an embodiment of the present invention is constituted of a closed loop, in which transmission loss is detected by the receiving apparatus 200 and the detected transmission loss is fed back to the

transmitting apparatus 100. Namely, the power of the optical signal output from the transmitting apparatus 100 can be self-controlled corresponding to the error detection signal transmitted from the receiving apparatus 200 without external control. Namely, the receiving apparatus 200 of the optical transmission system shown in FIG. 2 detects the transmission loss generated due to the change in transmission efficiency caused by the characteristics of the first optical fiber 185 and the receiving apparatus 200 and generates an error detection signal based on the transmission loss. Also, the transmitting apparatus 100 can keep the transmission efficiency uniform without external control by controlling the optical output power in the transmitting apparatus 100, corresponding to the error detection signal.

Also, since the optical transmission system according to the present invention keeps the transmission efficiency uniform, devices having large error allowance ranges can be used for the optical transmission system. Namely, the transmission efficiency of the optical transmission system deteriorates when devices have large error allowance ranges, the receiving apparatus 200 detects the transmission loss caused by the deterioration of the transmission efficiency and transmits the detected transmission loss. Since the transmitting apparatus 100 increases the optical output power according to the detected transmit loss, the deterioration of the transmission efficiency of the optical transmission system is prevented. It is therefore possible to reduce the cost of an optical transmission system since it is possible to use devices having large error allowance ranges.

Referring to FIG. 2, the transmitting apparatus 100 includes a parallel/serial data converter 110, a phase locked loop (PLL) 140, an error compensating driver 160, optical diodes 180 for transmission, and optical diodes 190 for reception.

The PLL 140 generates a first synchronized clock signal PLL\_CK1 synchronized with a predetermined clock signal CLK received from the input terminal CLK\_IN. The PLL 140 outputs the first synchronized clock signal PLL\_CK1 to the error compensating driver 160 as an actual clock signal for data transmission. The PLL 140 uses the clock signal CLK having a frequency of, for example, 25MHz through 162MHz as an input in

the case of high-speed transmission having a transmission speed on the GHz order. Also, the PLL 140 generates non-overlapping clock signals CKP and inverted non-overlapping clock signals for data serialization performed by the parallel/serial data converter 110, using the first synchronized clock signal PLL\_CK1. The PLL 140  
 5 outputs the generated non-overlapping clock signals CKP and inverted non-overlapping clock signals CKPB to the parallel/serial data converter 110. The PLL 140 will now be described in further detail below with reference to FIG. 3.

The parallel/serial data converter 110 serializes the input n-bit channel data in response to the non-overlapping clock signal CKP and the inverted non-overlapping  
 10 clock signal CKPB. Also, the parallel/serial data converter 110 outputs the converted serial channel data items to the error compensating driver 160. If parallel data is not converted into serial data, as many channels as the number of bits constituting the R/G/B color signals and as many channels as the number of bits constituting the control signal CON are required. For example, 36 channels are required in order to transmit  
 15 the R/G/B color signals and the control signal CON of nine bits in parallel in FIG. 2. However, when parallel data is converted into serial data and then, transmitted as in the present invention, it is possible to transmit the R/G/B color signals and the control signal CON of nine bits using four channels.

When the optical transmission system transmits graphic data as in an  
 20 embodiment of the present invention, the amount of data to be processed increases as the display screen size and resolution increases. Therefore, the frequency of the clock signal CLK for processing data increases and the transmission speed of the serialized data increases. Table 1 shows the frequency of the clock signal CLK according to resolution and the transmission speed of the serialized data according to the resolution,  
 25 when the input data is nine-bit parallel data.

Table 1

Resolution	Frequency of clock signal (CLK)	Transmission speed of serialized data
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640×480	25MHz	225Mbps
1024×768	65MHz	585Mbps
1280×1024	112MHz	1.008Gbps
1600×1200	162MHz	1.458Gbps

5 Referring to Table 1, the serialized data may need to be transmitted at high speeds on the GHz order according to the increase in the resolution. In general, a shift register realized by flip-flops is used as the parallel/serial data converter. When the parallel/serial data converter is realized using the flip-flops, it is not possible to process high speed data on the GHz order due to the holding and setting time of the flip-flop.

10 Therefore, the parallel/serial data converter is required to be realized by devices gated for a short time in order to process high speed data on the GHz order. The parallel/serial data converter 110 will be described in further detail below with reference to FIG. 6.

15 In FIG. 2, the optical diode 190 for reception can generally be realized by a photo diode. Also, the optical diode 190 for reception converts the error detection signal which is an optical signal received from the second optical fiber 195 into a current signal and outputs the current signal.

20 The error compensating driver 160 receives the serialized channel data items from the parallel/serial data converter 110 and the first synchronized clock signal PLL\_CK1 from the PLL 140 and converts the channel data items into a current signal. Also, the error compensating driver 160 changes the magnitude of modulation current or bias current, corresponding to the current signal converted by the optical diode for reception 190. Also, the error compensating driver 160 generates driving signals for driving the optical diodes for reception 180 by reflecting the modulation current and the bias current to a signal, in which the respective channel data are converted into current.

25 In FIG. 2, R\_DR, G\_DR, and B\_DR denote driving signals corresponding to the respective R/G/B color signals. CON\_DR and CLK\_DR denote driving signals

corresponding to the control signal CON and the clock signal CLK, respectively. The error compensating driver 160 will be described in further detail below with reference to FIG. 11.

The optical diodes 180 for transmission can generally be realized by laser diodes such as a vertical cavity surface emitting laser (VCSEL). Also, the optical diodes 180 for transmission output optical signals having optical output power corresponding to the respective driving signals output from the error compensating driver 160. In FIG. 2, R\_LD, G\_LD, and B\_LD denote the R/G/B color signals converted into optical signals, respectively. Also, CON\_LD and CLK\_LD denote the control signal CON and the clock signal CLK, which are converted into optical signals.

Referring to FIG. 2, the receiving apparatus 200 includes optical diodes 187 for reception, an optical diode for transmission 197, an error detection unit 210, a data recovery unit 250, and a phase locked loop (PLL) 260.

The optical diodes 187 for reception can be realized by the photo diodes as mentioned above. Also, the optical diodes 187 for reception receive optical signals transmitted through the first optical fiber 185 and convert the optical signals into current signals. In FIG. 2, R\_PD, G\_PD, and B\_PD denote the R/G/B signals converted into optical signals and transmitted through the first optical fiber 185. CON\_PD and CLK\_PD denote the control signal CON and the clock signal CLK, which are converted into optical signals and transmitted through the first optical fiber 185.

The error detection unit 210 converts the current signals received from the optical diodes 187 for reception into voltage signals and converts the voltage signals into digital signals. The digitized signals are output to the data recovery unit 250 and the PLL 260 as the recovered serial channel data and the recovered clock signal. In FIG. 2, R\_SRL, G\_SRL, B\_SRL, and CON\_SRL denote recovered serial channel data, respectively. Also, CLK\_SRL denotes a recovered clock signal. Also, the error detection unit 210 detects transmission loss caused by the first optical fiber 185 and the optical diodes 187 for reception from the received current signals in each channel. The detected transmission loss in each channel is encoded and converted into current in

response to the recovered clock signal CLK\_OUT and is output to the optical diode 197 for transmission. The error detection unit 210 will be described in further detail below with reference to FIG. 13.

The PLL 260 outputs a second synchronized clock signal, which is synchronized with the recovered clock signal CLK\_SRL generated by the error detection unit 210, as the recovered predetermined clock signal CLK\_OUT. Also, the PLL 260 generates non-overlapping clock signals CKP having a predetermined offset so as not to overlap each other, using the second synchronized clock signal CLK\_OUT and outputs the non-overlapping clock signals CKP to the data recovery unit 250. Here, the non-overlapping clock signals CKP are used for data recovery performed by the data recovery unit 250.

The data recovery unit 250 recovers the serial channel data recovered from the error detection unit 210 to channel data of n bits in response to the second synchronized clock signal CLK\_OUT. In FIG. 2, R\_OUT, G\_OUT, B\_OUT, and CON\_OUT denote the recovered R/G/B color signals and control signal CON of n bits, respectively.

The optical diode 197 for transmission can be realized by a laser diode. Also, the optical diode 197 for transmission converts the signal encoded and converted into current by the error detection unit 210 into an optical signal and outputs the converted optical signal as the error detection signal.

The optical signal transmission system according to an embodiment of the present invention converts the transmission loss detected by the receiving apparatus 200 into an optical signal and transmits the optical signal to the transmitting apparatus 100 through the second optical fiber. However, in FIG. 2, the second optical fiber 195 can be replaced by an electrical transmission line 193. In general, the transmission speed is higher in the optical fiber than in the electrical transmission line. Therefore, the optical transmission line is effective in transmitting channel data which must be transmitted at high speed. However, the error detection signal need not be transmitted at high speed as with the channel data. Therefore, the second optical fiber 195 for

transmitting the error detection signal can be replaced by the electrical transmission line 193.

When the second optical fiber 195 of FIG. 2 is replaced by the electrical transmission line 193, the structure of the optical transmission system shown in FIG. 2 changes. Namely, the optical diode 190 for reception is not used for the transmitting apparatus 100 and the optical diode 197 for transmission is not used for the receiving apparatus 200.

Also, when the second optical fiber 195 of FIG. 2 is replaced with the electrical transmission line 193, the operation of the optical transmission system shown in FIG. 2 changes.

The error detection unit 210 of the receiving apparatus 200 detects the transmission loss caused by the first optical transmission line 185 and the optical diodes 187 for reception and encodes channel information and the detected transmission loss into serial data. Also, the error detection unit 210 transmits the encoded data to the transmitting apparatus 100 through the electrical transmission line 193 as the error detection signal. Also, the error compensating driver 160 of the transmitting apparatus 100 receives the error detection signal transmitted through the electrical transmission line 193 and controls the optical output power, corresponding to the received error detection signal.

FIG. 3 is a block diagram showing the PLL 140 shown in FIG. 2. The PLL 140 includes a phase detector 142, a charge pump 144, a loop filter 148, and a voltage controlled oscillator (VCO) 146.

Referring to FIG. 3, the phase detector 142 compares the phase of a predetermined clock signal CLK received from an external source with the phase of a first non-overlapping clock signal CKP0 generated by the VOC 146, detects the phase difference, and outputs the detection result to the charge pump 144.

The charge pump 144 supplies electric charge to the loop filter 148 or sinks electric charge from the loop filter 148, corresponding to the phase difference detected by the phase detector 142.

In general, a low-pass filter is used as the loop filter 148, which receives electric charge from the charge pump 144 or sinks electric charge to the charge pump 144. A control voltage  $V_c$  is generated by the loop filter 146 receiving electric charge from the charge pump 144 or sinking electric charge to the charge pump 144.

5 The VCO 146 generates a signal having an oscillation frequency corresponding to the control voltage  $V_c$  as the first synchronized clock signal PLL\_CK1 synchronized with the predetermined clock signal CLK to the phase detector 142. Here, the first synchronized clock signal PLL\_CK1 is the first non-overlapping clock signal CKP0. Also, the VCO 146 generates first through  $n$ th overlapping clock signals CKP0 through  
 10 CKP $n-1$  having a predetermined offset so as not to overlap each other. Also, the VCO 146 inverts the first through  $n$ th overlapping clock signals CKP0 through CKP $n-1$  and generates inverted first through  $n$ th non-overlapping clock signals CKPB0 through CKPB $n-1$ . Here, the predetermined offset can correspond to the width of a unit bit, which will be described. The VCO 146 will now be described in detail with reference to  
 15 FIG. 4.

The PLL shown in FIG. 3 can be used as the PLL 260 of the receiving apparatus 200.

FIG. 4 is a circuit diagram showing the VCO 146 shown in FIG. 3. The VCO 146 includes first through ninth delay elements 300, 302, 304 . . . , 316. Here, for  
 20 convenience of explanation, the VCO 146 is mentioned to generate first through ninth overlapping clock signals CKP0 through CKP8 and inverted first through ninth non-overlapping clock signals CKPB0 through CKPB8.

Referring to FIG. 4, the VCO is formed of a ring oscillator using the nine delay elements 300, 302, 304 . . . , 316. The first through ninth non-overlapping clock signals CKP0 through CKP8 are output through the positive output terminals of the first through  
 25 ninth delay elements 300 through 316. The inverted first through ninth non-overlapping clock signals CKPB0 through CKPB8 are output through the respective negative output terminals of the first through ninth delay elements 300, 302, 304 . . . , 316. In the VCO shown in FIG. 4, the frequencies of the non-overlapping clock signals CKP0 through



CKP<sub>n-1</sub> generated by the respective delay elements 300, 302, 304 . . . , 316 can change as the delay time of the delay elements 300, 302, 304 . . . , 316 changes corresponding to the control voltage VC applied to the respective delay elements 300, 302, 304 . . . , 316.

FIG. 5 shows waveforms of the first through ninth non-overlapping clock signals CKP0 through CKP8 having a predetermined offset P18 and the first synchronized clock signal PLL\_CK1, which are output from the VCO shown in FIG. 4.

FIG. 6 is a block diagram showing the parallel/serial data converter 110 shown in FIG. 2. The parallel/serial data converter 110 includes a data latch 700 and a data serializer 750.

FIGS. 7A and 7B show waveforms of the operation of the apparatus shown in FIG. 6. FIG. 7A shows the first synchronized clock signal PLL\_CK1. FIG. 7B shows the serial channel data DOUT output through the data serializer 750 of FIG. 6.

Referring to FIGS. 6 and 7, the data latch 700 receives n-bit channel data through an input terminal DIN, segments the n-bit channel data by N bits in response to the first through mth latch clock signals CKL0 through CKL<sub>m-1</sub> having a timing margin corresponding to N (N is a positive integer greater than or equal to 2) unit bits among the first through nth non-overlapping clock signals CKP0 through CKP<sub>n-1</sub> and latches the segmented channel data. Here, the first latch clock signal CKL0 is the non-overlapping clock signal having the greatest timing margin with respect to the first synchronized clock signal PLL\_CK1. The reason why the first latch clock signal CKL0 is selected as the non-overlapping clock signal having the largest timing margin with respect to the first synchronized clock signal PLL\_CK1 and the detailed operation of the latch 700 will be described below with reference to FIGS. 8 and 9. In FIG. 6, the n-bit channel data input to the input terminal DIN can be the R/G/B color signals or the control signal CON.

The data serializer 750 receives the n-bit channel data latched by the data latch 700, the first through nth overlapping clock signals CKP0 through CKP<sub>n-1</sub> and the inverted first through nth non-overlapping clock signals CKPB0 through CKPB<sub>n-1</sub> and

performs a logic operation on the received channel data and signals. Also, the data serializer 750 outputs the logic operation result as the serial channel data shown in FIG. 7B through the output terminal DOUT. Here, P18 denotes a unit bit width. The data serializer 750 will be described in detail below with reference to FIG. 10.

5           The apparatus shown in FIG. 6 will now be described, assuming that  $n$  is 9 and  $N$  is 3.

FIG. 8 is a circuit diagram showing the latch 700 shown in FIG. 6. The data latch 700 includes a first latch 710 including flip-flops 710a through 710i, a second latch 720 including flip-flops 720a through 720 f, and a third latch 730 including flip-flops 730a through 730c.

FIGS. 9A through 9H show main waveforms in the operation of the data latch shown in FIG. 8. FIG. 9A shows the first non-overlapping clock signal CKP0. FIG. 9B denotes channel data of nine bits input to the first latch 710. FIG. 9C shows the first latch clock signal CKL1 for controlling the operation of the first latch 710. FIG. 9D shows channel data latched by the first latch 710. FIG. 9E shows a second latch clock signal CKL2 for controlling the operation of the second latch 720. FIG. 9F shows the channel data latched by the second latch 720. FIG. 9G shows a third latch clock signal CKL3 for controlling the operation of the third latch 730. FIG. 9H shows the channel data latched by the third latch 730. FIG. 9I shows the result of serializing the data latched by the data latch shown in FIG. 8 by the data serializer 750 (refer to FIG. 6).

Referring to FIGS. 8 and 9, the nine flip-flops 710a through 710i included in the first latch 710 correspond to the respective bits of the nine-bit channel data. Namely, the flip-flops 710a through 710i receive the respective bits of the channel data generated in response to the first non-overlapping clock signal CKP0 to input terminals D, as shown in FIG. 9B. Here, D[8] through D[0] denote the respective bits of the nine-bit channel data. Also, the flip-flops 710a through 710i latch input channel data in response to the first latch clock signal CKL0. As mentioned above, the first latch clock signal CKL0 has the largest timing margin with respect to the first non-overlapping clock signal CKP0 shown in FIGS. 5B and 9A among the first through ninth non-overlapping

clock signals CKP0 through CKP8 (see FIG. 5). Therefore, the sixth non-overlapping clock signal CKP5 having a nearly inverted phase with respect to the phase of the first non-overlapping clock signal CKP0 can be used as the first latch clock signal CKL0. Namely, the first latch 710 latches input channel data in response to the sixth non-overlapping clock signal CKP5. Also, upper three bits of the channel data latched by the first latch 710 are latched and lower six bits are output to the second latch 720. Here, Do[8], Do[7], and Do[6] denote the upper three bits of the channel data latched by the first latch 710.

The first latch 710 can stably latch Dn[8:6] in the nine-bit channel data shown in FIG. 9B by using the sixth non-overlapping clock signal CKP5 shown in FIG. 9C as the first latch clock signal CKL0.

The six flip-flops 720a through 720f included in the second latch 720 correspond to the flip-flops 710d through 710i included in the first latch 710. Namely, the flip-flops 720a through 720f receive the data output from the flip-flops 710d through 710i to the input terminals D in response to the sixth non-overlapping clock signal CKP5, as shown in FIG. 9C. Also, the flip-flops 720a through 720f latch the input data in response to the second latch clock signal CKL1. As mentioned above, second latch clock signal CKL1 has a timing margin corresponding to three unit bits with respect to the first latch clock signal CKL0. Therefore, the sixth non-overlapping clock signal CKP5 used as the first latch clock signal CKL0 and the ninth non-overlapping clock signal CKP8 having the timing margin of three unit bits can be used as the second latch clock signal CKL1. Namely, the second latch 720 latches the input data in response to the ninth non-overlapping clock signal CKP8. The upper three bits of the channel data latched by the second latch 720 are latched and the lower three bits are output to the third latch 730. Here, Do[5], Do[4], and Do[3] denote the upper three bits of the latched data.

The second latch 720 can stably latch Dn[5:3] in the nine-bit channel data shown in FIG. 9D by using the ninth overlapping clock signal CKP8 shown in FIG. 9E as the second latch clock signal CKL1.

The three flip-flops 730a through 730c included in the third latch 730 correspond to the flip-flops 720d through 720f included in the second latch 720. Namely, the flip-flops 730a through 730c receive data output from the flip-flops 720d through 720f in response to the ninth non-overlapping clock signal CKP8 to the input terminals D, as shown in FIG. 9E. Also, the flip-flops 730a through 730c latch the input data in response to the third latch clock signal CKL2. As mentioned above, the third latch clock signal CKL2 has a timing margin corresponding to the three unit bits with respect to the second latch clock signal CKL1. Therefore, the third non-overlapping clock signal CKP2 having a timing margin of three unit bits with respect to the ninth non-overlapping clock signal CKP8 used as the second latch clock signal CKL1 can be used as the third latch clock signal CKL2. Namely, the third latch 730 latches the input data and outputs the latched data in response to the third non-overlapping clock signal CKP2. Here, Do[2], Do[1], and Do[0] denote the channel data output from the third latch 730.

The third latch 730 can stably latch Dn[2:0] in the six-bit channel data shown in FIG. 9F by using the third non-overlapping clock signal CKP2 shown in FIG. 9G as the third latch clock signal CKL2.

FIG. 10 is a circuit diagram showing the data serializer 750 shown in FIG. 6. The data serializer 750 includes a first logic operator 760 including NAND gates 760a through 760i, a second logic operator 762 including NAND gates 762a through 762c, and a third logic operator 764 including a NAND gate 766 and an inverter 768.

Referring to FIGS. 9 and 10, the nine NAND gates 760a through 760i included in the first logic operator 760 correspond to the respective bits of the nine-bit channel data latched by the data latch (refer to FIG. 6). Also, the NAND gates 760a through 760i correspond to the first through ninth non-overlapping clock signals CKP0 through CKP8, respectively, and the inverted second through inverted first non-overlapping clock signals CKPB2 through CKPB1, respectively. Namely, the NAND gates 760a through 760i receive the respective bits corresponding to the latched nine-bit channel data and the non-overlapping clock signals and the inverted non-overlapping clock signals corresponding thereto and perform a logic operation on the received bits and

signals. For example, the NAND gate 760a receives  $Dn[8]$  which is the most significant bit (MSB) among the nine-bit channel data, the first non-overlapping clock signal CKP0, and the inverted second non-overlapping clock signal CKPB1 and performs a NAND operation on the received bit and signals. Therefore, the NAND gate 760a generates  
 5 inverted channel data  $\overline{Dn[8]}$  during a first period P1, where the first non-overlapping clock signal CKP0 and the inverted second non-overlapping clock signal CKPB1 are simultaneously transited to a logic high level. The remaining NAND gates 760b through 760i output data of the logic high level during the first period P1. Also, the NAND gate 760b receive  $Dn[7]$  among the nine-bit channel data, the second non-overlapping clock  
 10 signal CKP1, and the inverted third non-overlapping clock signal CKPB2 and performs a NAND operation on the received bit and signals. Therefore, the NAND gate 760b generates inverted channel data  $\overline{Dn[7]}$  during a second period P3, where the second non-overlapping clock signal CKP1 and the inverted third non-overlapping clock signal CKPB2 are simultaneously transited to the logic high level. The remaining NAND gates  
 15 760a and 760c through 760i output data of a logic high level during the second period P3. The NAND gate 760c through 760i output inverted channel data  $\overline{Dn[6]}$  through  $\overline{Dn[0]}$  during third through ninth periods P5 through P9.

The NAND gate 762a of the second logic operator 762 performs a NAND operation on the data output from the NAND gates 760a through 760c. The NAND gate  
 20 762b performs a NAND operation on the data output from the NAND gates 760d through 760f. The NAND gate 762c performs a NAND operation on the data output from the NAND gates 760g through 760i.

The NOR gate 766 of the third logic operator 764 receives the data on which a NAND operation is performed by the NAND gates 762a through 762c and performs a  
 25 NOR operation on the data. The inverter 768 inverts the data on which a NOR operation is performed by the NOR gate 766 and outputs the inversion result through the output terminal DOUT as the serial channel data. The serial channel data shown in FIG. 9I is output to the output terminal DOUT.

Referring to FIGS. 8, 9, and 10, the data serializer shown in FIG. 10 serializes the upper three bits,  $Dn[8]$ ,  $Dn[7]$ , and  $Dn[6]$  among the channel data  $Dn[8:0]$  shown in FIG. 9D and outputs the serialized upper three bits, during the first through third periods P1 through P3. Namely, the upper three bits can be stably serialized in the center of the channel data  $Dn[8:0]$  shown in FIG. 9D. The data serializer shown in FIG. 10 serializes the channel data  $Dn[2:0]$  shown in FIG. 9H and outputs the serialized channel data during seventh through ninth periods P13 through P17. Namely, the three lower bits can be stably serialized in the center of the channel data  $Dn[2:0]$  shown in FIG. 9H.

It is assumed that the data latch shown in FIG. 8 latches the nine-bit channel data by a general method, in which the first synchronized clock signal  $PLL\_CK1$  is used, without segmenting and latching the nine-bit channel data. The data serializer shown in FIG. 10 outputs the MSB  $Dn[8]$  of the channel data shown in FIG. 9B as the serial channel data in the first period P1. Also, the data serializer shown in FIG. 10 outputs the least significant bit (LSB)  $Dn[0]$  of the channel data shown in FIG. 9B as the serial channel data in the ninth period P8. At this time, the data serializer can output incorrect serial channel data even when a slight phase difference exists between the first synchronized clock signal  $PLL\_CK1$  shown in FIG. 9A and the nine-bit channel data shown in FIG. 9B. Namely, the data serializer shown in FIG. 10 can output the LSB  $Dn-1[0]$  of the previous channel data at a point in time where the MSB  $Dn[8]$  must be output as the serial channel data. Also, the data serializer can output the MSB  $Dn+1[8]$  of the next channel data at the point in time where the LSB  $Dn[0]$  must be output as the serial channel data. As a result, the LSB of the previous channel data or the MSB of the next channel data can be mixed at the boundary of the channel data.

However, since the data latch shown in FIG. 9 segments and latches the nine-bit channel data using the sixth, ninth, and third overlapping clock signals  $CKP5$ ,  $CKP8$ , and  $CKP2$ , the data serializer shown in FIG. 10 can stably serialize the nine-bit channel data in the center of the parallel channel data.

Since the data serializer shown in FIG. 10 is realized only by gates gated for a short time, a high-speed serializer of a level greater than the GHz level can be realized

and the size of a circuit can be significantly reduced compared with the circuit in the conventional general data serializer realized by flip-flops. Also, since the data serializer shown in FIG. 10 serializes data using the non-overlapping clock signals CKP whose frequencies are lower than the frequencies of the conventional data serializer, it is possible to reduce power consumption. For example, the conventional data serializer serializes data using a clock signal multiplied by the number of bits of the parallel data.

FIG. 11 is a block diagram showing the error compensating driver 160 shown in FIG. 2. The error compensating driver 160 includes first through fifth signal drivers 168 through 176, an output controller 166, a transmission error compensator 164, and an error detection receiver 162. Also, in FIG. 11, optical diodes for transmission 180a through 180e and an optical diode for reception 190 are shown together for convenience of explanation. In FIG. 11, R\_SRL, G\_SRL, B\_SRL, and CON\_SRL denote the serial channel data output from the parallel/serial data converter 110 shown in FIG. 2. PLL\_CK1 denotes the first synchronized clock signal output from the PLL 140 shown in FIG. 2.

Referring to FIG. 11, the optical diode for reception 190 receives an error detection signal, which is converted into an optical signal and transmitted by the receiving apparatus 200 (refer to FIG. 2) to the transmitting apparatus and converts the received error detection signal into current. As mentioned above, channel information and information on the transmission loss detected in each channel are included in the error detection signal.

The error detection receiver 162 receives the signal converted into current from the optical diode for reception 190 and converts the received signal into a voltage. Also, the error detection receiver 162 digitizes the converted voltage signal, and outputs the digitized signal to the transmission error compensator 164 as an error compensating signal.

The transmission error compensator 164 decodes the error compensation signal output from the error detection receiver 162 in response to the first synchronized clock signal PLL\_CK1. Namely, the transmission error compensator 164 decodes the error

compensation signal and recovers the transmission loss data in each channel, which is detected by the receiving apparatus 200 (see FIG. 2). The transmission error compensator 164 analog converts the recovered transmission loss data. The analog converted signal is output to the optical output controller 166 as the transmission loss compensation signal for compensating for transmission loss generated in each channel. The transmission error compensator 164 will be described in detail below with reference to FIG. 12.

The output controller 166 receives the transmission error compensation signals generated by the transmission error compensator 164, generates optical output control signals corresponding to the transmission loss compensation signals, and outputs the optical output control signals to the first through fifth signal drivers 168, 170, 172, 174 and 176. Here, the optical output control signals are control signals for controlling the modulation current or the bias current of the first through fifth signal drivers 168, 170, 172, 174 and 176. The modulation current is for changing the swing range of an actually transmitted optical signal. The bias current is for controlling the direct current (DC) level of the output optical signal. The bias current is set at the on/off boundary of the optical diode for transmission and prevents the transmission speed of data from deteriorating according to whether the optical diode for transmission is turned on/off.

The first through fifth signal drivers 168, 170, 172, 174 and 176 convert the serial channel data received to each channel into current signals. Also, the first through fifth signal drivers 168, 170, 172, 174 and 176 change the magnitude of the bias current or the modulation current in response to the optical output control signal output from the optical output controller 166. Here, whether the first through fifth signal drivers 168, 170, 172, 174 and 176 change the bias current or the modulation current in response to the optical output control signal is determined by the error detection signal transmitted from the receiving apparatus 200 (see FIG. 2). Also, the first through fifth signal drivers 168, 170, 172, 174 and 176 add the converted current signal, the bias current, and the modulation current to each other and outputs the addition result as a driving signal for driving the corresponding optical diodes 180a through 180e for transmission.



The optical diodes 180a through 180e for transmission generate an optical signal having an optical output power corresponding to the driving signal output from the first through fifth signal drivers 168, 170, 172, 174 and 176.

The driving signals for driving the optical diodes 180a through 180e for transmission change corresponding to the error detection signal detected by the receiving apparatus. Transmission loss generated during transmission from the transmitting apparatus to the receiving apparatus is compensated in the optical signal output from the optical diodes 180a through 180e for transmission.

In FIG. 2, when the second optical fiber 195 is replaced by the electrical transmission line 193, the structure of the error compensating driver shown in FIG. 11 changes. Namely, in FIG. 2, when the second optical fiber 195 is replaced by the electrical transmission line 193, the error detection receiver 162 is not used for the error compensating driver. In the error compensating driver, the error detection signal transmitted from the electrical transmission line 193 is directly received by the transmission error compensator 164. After the transmission error compensator 164 receives the error detection signal from the electrical transmission line 193, the operations of the transmission error compensator 164, the output power controller 166, and the first through fifth signal drivers 168 through 176 were described above with reference to FIG. 11.

FIG. 12 is a block diagram showing the transmission error compensator 164 shown in FIG. 11. The transmission error compensator 164 includes a decoder and a digital-to-analog converter (DAC) 182.

Referring to FIG. 12, the decoder 180 decodes the error compensation signal output from the error detection receiver 162 (see FIG. 11) in response to the first synchronized clock signal PLL\_CK1. The decoding result is output to the DAC 182 as the transmission loss data generated when each channel data is transmitted. In FIG. 12, ERR\_IN denotes the error compensation signal output from the error detection receiver 162. R\_ERR, G\_ERR, and B\_ERR denote the transmission error data detected by the channel, to which the R/G/B color signals are transmitted. CON\_ERR

and CLK\_ERR denote the transmission loss data detected by the channel, to which the control signal CON and the clock signal CLK are transmitted.

The DAC 182 converts the transmission loss data output from the decoder 180 into analog signals as the transmission loss compensating signals for compensating for loss in each channel. In FIG 12, RLS\_OUT, GLS\_OUT, and BLS\_OUT denote transmission loss compensation signals for compensating for the transmission loss of each of the R/G/B color signals. CONLS\_OUT and CLKLS\_OUT denote transmission loss compensation signals for compensating for the transmission loss of the control signal CON and the clock signal CLK.

FIG. 13 is a block diagram showing the error detection unit 210 shown in FIG. 2. The error detection unit 210 includes first through fifth signal receivers 212, 214, 216, 218 and 220, an error detection signal driver 224, and a transmission error detector 222. Also, in FIG. 13, the optical diodes 187a through 187e for reception and the optical diode 197 for transmission are shown together for convenience of explanation.

Referring to FIG. 13, the optical diodes 187a through 187e for reception receive the channel data converted into the optical signals through the first optical fiber 185 (see FIG. 2). The optical diodes 187a through 187e for transmission convert the received optical signals into current signals and output the current signals.

The first through fifth signal receivers 212, 214, 216, 218 and 220 convert the current signals received from the optical diodes 187a through 187e for reception into voltage signals and the converted voltage signals to the transmission error detector 222. At this time, the voltage signals output from the first through fifth signal receivers 212, 214, 216, 218 and 220 are voltage signal pairs whose phases are inverted from each other. Also, the first through fifth signal receivers 212, 214, 216, 218 and 220 convert the levels of the converted voltage signals and output the digitalized signals as the recovered serial channel data and the recovered clock signal. In FIG. 13, R\_REC, G\_REC, B\_REC, and CON\_REC denote the recovered serial channel data and CLK\_REC denotes the recovered clock signal.

The transmission error detector 222 receive the converted voltage signal pairs from the first through fifth signal receivers 212, 214, 216, 218 and 220 and detect the transmission loss in each channel using the voltage signal pairs. Here, two methods are used for obtaining transmission loss in each channel. In the first method, the transmission error detector 222 selects one voltage signal among the voltage signal pairs and obtains the transmission loss by detecting the amplitude of the selected voltage signal. For example, when the optical transmission system keeps the transmission efficiency uniform, the level of the voltage signal converted by the first through fifth signal receivers 212, 214, 216, 218 and 220 will keep a predetermined reference level. However, when the transmission efficiency changes due to the characteristics of the first optical fiber 185 and the receiving apparatus 200 and thus, transmission loss is generated, the level of the voltage signal converted by the first through fifth signal receivers 212, 214, 216, 218 and 220 deviates from a first predetermined reference level. The transmission error detector 222 detects the level of the converted voltage level and compares the level of the detected voltage signal with the first predetermined level. Accordingly, transmission loss is detected. The transmitting apparatus 100 (see FIG. 2) controls the modulation current, corresponding to the detected transmission error. Therefore, the level of the voltage signal converted by the first through fifth signal receivers 212, 214, 216, 218 and 220 of the receiving apparatus (see FIG. 2) 200 is kept at the first predetermined reference level.

In the second method, the average levels of each of the voltage signal pairs are obtained and the transmission error is obtained using the difference between the average levels. When transmission loss is not generated, the difference between the average levels will be kept at a predetermined second reference level. However, when transmission loss is generated, the difference between the average levels will deviate from the second reference level. The transmission error detector 222 can detect transmission loss by comparing the difference between the average levels of each of the voltage signal pairs with the second reference level. Also, the transmitting apparatus 200 controls the bias current, corresponding to the detected transmission

loss. Therefore, the difference between the average levels of each of the voltage signal pairs converted by the first through fifth signal receivers 212 through 220 can be kept at the second reference level.

Also, the transmission error detector 222 encodes the obtained transmission loss of each channel as transmission loss data having channel information and transmission loss information in response to the second synchronized clock signal CLK\_OUT and outputs the encoded transmission loss. The transmission error detector 222 will be described in detail below with reference to FIGS. 14 and 15.

The optical driver 224 receives the transmission loss data output from the transmission error detector 222 and converts the received transmission loss data into a current signal and outputs the converted direct signal as a driving signal for driving the optical diode 197 for transmission.

The optical diode 197 transmission converts the direct signal converted by the optical driver 224 into an optical signal and outputs the converted optical signal as an error detection signal.

In FIG. 2, when the second optical fiber 195 is replaced by the electrical transmission line 193, the structure of the error detection receiver shown in FIG. 13 changes. Namely, in FIG. 2, when the second optical fiber 195 is replaced with the electrical transmission line 193, the error detection signal driver 224 is not used for the error detection unit. Namely, the transmission error detector 222 of the error detection unit outputs encoded data as an error detection signal and the error detection signal is transmitted to the transmitting apparatus 100 through the electrical transmission line 193.

FIG. 14 is a block diagram showing an embodiment of the transmission error detector 222 shown in FIG. 13. The transmission error detector 222 includes an amplitude detector and comparator 230, an analog-to-digital converter (ADC) 232, and an encoder 234.

Referring to FIG. 14, the amplitude detector and comparator 230 selects one voltage signal among the voltage signal pairs output from the first through fifth signal

receivers 212, 214, 216, 218 and 220 (see FIG. 13) and detects the amplitude of the voltage signal. In FIG. 14, RVL\_P/RVL\_N, GVL\_P/GVL\_N, and BVL\_P/BVL\_N denote the voltage signal pairs generated by the first through third optical receivers 212, 214 and 216. CONVL\_P/CONVL\_N and CLKVL\_P/CLKVL\_N denote the voltage signal pairs generated by the fourth and fifth signal receivers 218 and 220. Also, the amplitude detector and comparator 230 compares the detected amplitude with a first reference voltage  $V_{ref1}$  and outputs the comparison result as the detected transmission loss to the ADC 232.

The ADC 232 receives transmission losses of each channel from the amplitude detector and comparator 230 and converts the received transmission losses of each channel into digital signals in response to the second synchronized clock signal CLK\_OUT and outputs the converted transmission loss in digital form.

The encoder 234 receives the digital signals output from the ADC 232 to each channel in response to the second synchronized clock signal CLK\_OUT and encodes the digital signals to digital signals having channel information and error information. Also, the encoder 234 outputs encoded data to the error detection signal driver 224 (see FIG. 13) as error detection data. In FIG. 14, ERR\_DT denotes the error detection data output from the encoder 234.

FIG. 15 is a block diagram showing another embodiment of the transmission error detector 222 shown in FIG. 13. The transmission error detector 222 includes first through fifth signal detectors and comparators 240, 242, 244, 246 and 248, an ADC 260, and an encoder 270.

Referring to FIG. 15, the first signal detector and comparator 240 receives the voltage signal pairs RVL\_P and RVL\_N output from the first signal receiver 212 (refer to FIG. 13) and obtains the difference between the average levels of each of the received voltage signal pairs. Also, the first signal detector and comparator 240 compares the difference between the average levels with a second reference voltage  $V_{ref2}$  and outputs the comparison result as the transmission loss to the ADC 260. Since the second through fifth signal detectors and comparators 242 and 248 perform the same

operations as the operation performed by the first signal detector and comparator 240, detailed descriptions thereof will be omitted.

The ADC 260 receive the transmission loss output from the first through fifth signal detectors and comparators 240, 242, 244, 246 and 248 and digitally converts the received transmission loss in response to the second synchronized clock signal CLK\_OUT, and outputs the converted transmission loss in digital form.

The encoder 270 receives the digital signals output from the each channel of the ADC 260 and encodes the received digital signals to a digital signal having channel information and error information in response to the second synchronized clock signal CLK\_OUT. Also, the encoder 234 outputs the encoded data as error detection data ERR\_DT to the error detection signal driver 224 (see FIG. 13).

While this invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

In the optical transmission system for compensating for transmission loss according to the present invention, the receiving apparatus detects transmission loss and transmits the detected transmission loss to the transmitting apparatus and the transmitting apparatus controls the optical output power, corresponding to the transmission loss transmitted from the receiving apparatus. Accordingly, it is possible to keep the optical efficiency uniform without the need for external control. Therefore, since a standard device, where the error allowance range is large, can be used, it is possible to reduce costs. Also, because the parallel/serial data converter is realized in a gate-oriented configuration, it is possible to convert data at high speeds greater than the GHz level and to reduce the size of the circuit. Also, it is possible to reduce power consumption since the non-overlapping clock signals whose frequencies are relatively low are used even when data is converted at high speeds greater than the GHz level.

## **OPTICAL TRANSMISSION SYSTEM FOR COMPENSATING FOR TRANSMISSION LOSS**

### Abstract of the Disclosure

5 An optical transmission system for compensating for transmission loss includes a transmitting apparatus for serializing a plurality of  $n$  ( $n$  is a natural number)-bit channel data received from the outside in response to a predetermined clock signal, converting the serialized channel data and the predetermined clock signal into a current signal whose magnitude changes corresponding to an error detection signal, and outputting optical signals having optical output power corresponding to the magnitude of the current signal, a first optical fiber for transmitting the optical signals, a receiving apparatus for recovering the  $n$ -bit channel data and the predetermined clock signal from the optical signals received through the first optical fiber, detecting transmission loss generated when the optical signals are transmitted and received, optically converting the transmission loss, and outputting the optically converted transmission loss as the error detection signal, and a second optical fiber for transmitting the optical converted error detection signal to the transmitting apparatus. Since the receiving apparatus and the transmitting apparatus forms a closed loop, it is possible to keep optical efficiency uniform, corresponding to the transmission loss transmitted by the receiving apparatus. Also, the parallel/serial data converter is realized by the gate, it is possible to convert data at high speeds of greater than the GHz level and to reduce the size of the circuit. Also, it is possible to reduce power consumption since the non-overlapping clock signals whose frequencies are relatively low are used even when data is converted at high speeds greater than the GHz level.

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